

The Role of the Parasitic Capacitance of the Inductor in Boost Converters with Normally-On SiC JFETs

Mariusz Zdanowski

Institute of Control and Industrial Electronics
Warsaw University of Technology
Warsaw, Poland
mariusz.zdanowski@ee.pw.edu.pl

Jacek Rabkowski, Konstantin Kostov, Hans Peter-Nee

Electrical Energy Conversion (E2C) Laboratory
School of Electrical Engineering
KTH Royal Institute of Technology
Stockholm, Sweden

Abstract—In this paper the impact of the parasitic capacitance of the inductor on the performance of a fast-switching boost converters with SiC JFETs is discussed. Two inductor designs, one conventional and another with a space between the winding layers, are investigated and their parasitic capacitances are measured by different methods. The air-gap between the winding layers reduced the inductor self-capacitance more than 8 times. The two inductors were used in a 2 kW, 100 kHz boost converter with a normally-on SiC JFET and their performance was compared. When the inductor with a low self-capacitance was used, there were fewer oscillations during the switching transients and the losses were reduced about 16 %.

Keywords – parasitic capacitance; inductor design; DC-DC converter; Silicon Carbide, JFET

I. INTRODUCTION

The introduction of *Silicon Carbide* (SiC) power transistors has a significant impact on the performance of power electronic converters. The four types of SiC devices available on the market - the normally-on [1]-[2] and normally-off [3]-[4] JFETs, BJT [5], and MOSFET [6], all have low parasitic capacitance values and fast switching capabilities. This contributes to substantial reduction of the switching energies in comparison to their Si-based counterparts, which was shown in a number of publications [7]-[16]. Limited switching power losses lead to reduced cooling requirement and smaller heatsinks. Also, with higher switching frequency the ripple requirements can be met with smaller passive components. Thus, converters with SiC devices are smaller, lighter, and have higher power density. On the other hand, very fast switching transitions increase the importance of parasitic elements like the self-capacitance of inductors, which may have a substantial impact on the switching behavior of the devices.

In this paper a fast-switching normally-on SiC JFET boost converter is examined with special focus on the input inductor design. Although the parasitic capacitance of an inductor is distributed between the winding turns (turn-to-turn capacitance), winding layers (layer-to-layer capacitance), and between the winding and the core of the inductor (winding-to-core capacitance), a simplified model with a lumped parasitic capacitance is usually sufficient for modeling the high-frequency behavior of the inductor and its impact on the converter. Recharging the parasitic capacitance during the

switching process has a negative influence on the shape of the current waveforms and power losses of the converter. At least four papers [17]-[20] describe the role of the parasitic capacitance of inductors and present methods to evaluate it. They conclude that single-layer inductors have the lowest parasitic capacitance, which is not surprising, because they do not have layer-to-layer capacitance. It is, therefore, beneficial to use such inductors in fast switching converters, but that may be impossible when the required inductance is high or the core has a small cross-section. This is why the authors of this paper propose a new multilayer winding method, which minimizes the self-capacitance of the inductor. Two double-layer inductors are compared – one with the conventional winding and another with the newly proposed one. The self-capacitance of both inductors was measured by different methods and the new type of winding was found to reduce the parasitic capacitance more than eight times. Then the two inductors were used in a 2 kW boost converter with fast-switching SiC JFET. The comparison shows that the converter with low-capacitance inductor has fewer switching oscillations and lower losses.

II. INDUCTOR DESIGN

Two different inductors with the same ratings: $L = 1.2$ mH and $I_{max} = 8$ A, are investigated in this paper. Both inductors have the same core UI93, material N87, and number of turns $N = 40$, calculated from

$$N = \frac{L \cdot I_{L,pp}}{B_{pp} \cdot A_e}, \quad (1)$$

where $I_{L,pp}$ and B_{pp} denote the peak-to-peak values of the inductor current and induction respectively, and A_e is the effective cross sectional area of the core, given in core's datasheet (840 mm² in this case).

In order to reduce the eddy currents and winding losses at the operating frequency of 100 kHz, a Litz copper wire, consisting of 120 strands with 0.1 mm diameter each, has been used. The skin depth (δ) can be calculated from

$$\delta = \sqrt{\frac{2\rho_c}{\mu\omega}}, \quad (2)$$

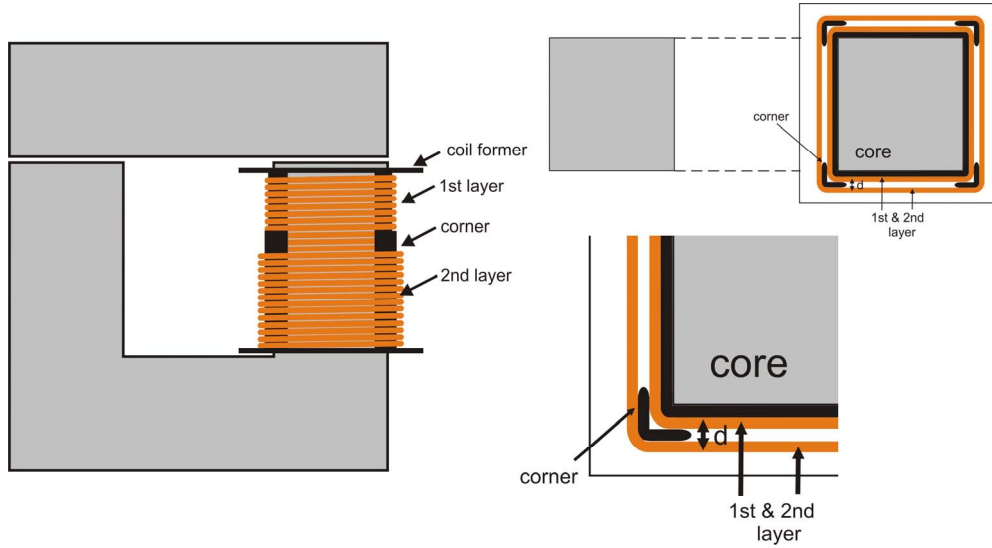


Figure 1. Layout of the optimized, low self-capacitance inductor No. 2.

where ρ_c is the electrical resistivity of the conducting material (for copper it is $23 \cdot 10^{-9} \Omega \text{m}$ at 100°C), μ is the permeability of the material (for copper $\mu \approx \mu_0$), and $\omega = 2\pi f$, is the angular frequency. With these values the penetration depth is approximately 0.241 mm.

Although the windings of the inductors have the same number of turns and both have two layers, there is different space between the layers. The first inductor (No. 1) has been wound using the typical winding method, with 0.2 mm insulation tape between the layers. The second inductor (No. 2) has spacers inserted between the winding layers as shown in Fig. 1, which increases the distance between the layers, and thus, reduce the layer-to-layer parasitic capacitance. The spacers, made of TECAVINYL PVC material, have low relative permittivity, $\epsilon_r = 3$, and maximum operating temperature of 100°C . They provide a distance of $d = 3 \text{ mm}$ between the winding layers. Therefore, the insulation material is mostly air with a relative permittivity close to unity.

Both inductors have 1.4 mm air-gap in the core.

III. SELF-CAPACITANCE MEASUREMENT METHODS

The self-capacitance of both inductors, No. 1 and No. 2, was measured in four different ways. Three of the four measurement methods [19]-[21] use an oscilloscope, and therefore, the capacitance of the probe must be taken into account. To confirm the results the impedance of the inductors was measured also with a *vector network analyzer* (VNA).

A. Method A: Frequency Scanning

The parasitic capacitance of the inductor can be measured easily by frequency scanning [22]. The inductance L of the inductor is measured with an *RLC*-meter for a given frequency. When variable frequency voltage is applied to the inductor (Fig. 2a), its parasitic capacitance C will cause a parallel resonance. The resonant frequency f_r can be detected by the maximum amplitude of the voltage across the inductor (Fig. 2b). Resistor R limits the current drawn from the AC

source – it is not part of the inductor. The parasitic capacitance can be calculated from

$$C = \frac{1}{4\pi^2 f_r^2 L}. \quad (3)$$

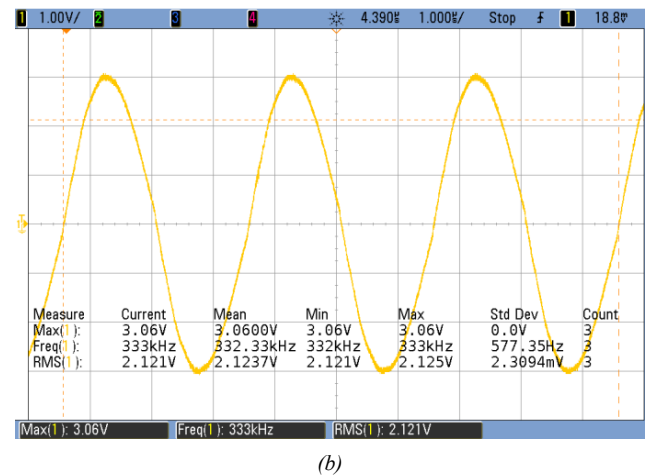
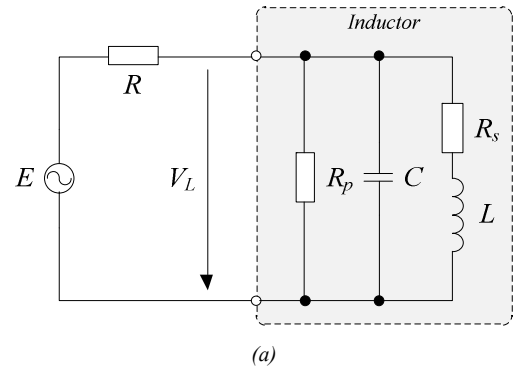


Figure 2. Test setup for the frequency scanning (a) and waveform of inductor voltage during resonance (b).

B. Method B: Self-Oscillation Excitation

The second measurement method is also based on parallel resonance, but unlike the previous method, it uses a single-pulse excitation [19]. The inductor current is interrupted by a transistor switch (Fig. 3a) resulting in a self-damped oscillation (Fig. 3b). The method requires at least two measurements – one with a single switch and another one with two switches in parallel. If the two switches are identical, it can be assumed that they have the same parasitic capacitances (C_{JFET}), which is added to the parasitic capacitance of the inductor (C). In addition, there is the capacitance of the voltage probe (C_p). By measuring the period of the oscillations and knowing the inductance L , the total capacitances (C_1 and C_2) of the resonant circuits during the two measurements can be calculated. Because the parasitic capacitances in each measurement are in parallel, the following equations apply:

$$\begin{aligned} C_1 &= C + C_p + C_{JFET} \\ C_2 &= C + C_p + 2C_{JFET} \end{aligned} \quad (4)$$

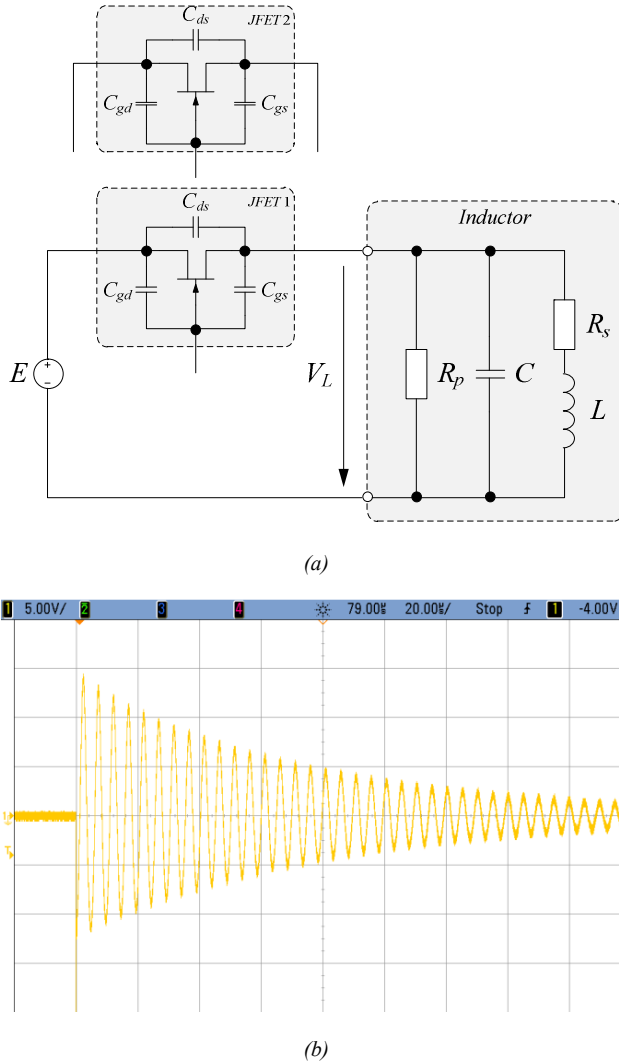


Figure 3. Test setup for the frequency scanning (a) and waveform of inductor voltage during resonance (b).

Then the parasitic capacitance of the inductor is

$$C = 2C_1 - C_2 - C_p. \quad (5)$$

There is some uncertainty in the measurement due to the tolerances in the parasitic capacitances of the switches. The C_{JFET} value in (4) is actually the average of the parasitic capacitances of the two switches used in the measurements. It is possible to reduce the error caused by the tolerances by making more measurements and adding more switches in parallel, but that would require more time and effort.

C. Method C: Parasitic Charge Measurement

The third method is based on measurements of the inductor current peaks during the operation of the boost converter. At transistor turn-on and turn-off the parasitic capacitance is recharging, which leads to current spikes as in Fig. 4. According to [20]-[21] the stray capacitance can be approximated by

$$C = I_L \frac{\Delta t}{\Delta V}, \quad (6)$$

where I_L is the peak value of the inductor current spike, ΔV is the voltage step applied to the inductor and Δt is the duration of the spike.

D. Method D: Network Analyzer

The results obtained by methods A-C were verified with a VNA. It measures the s-parameters of the equipment under test. The impedance vs. frequency characteristic of the inductor can be calculated from its s-parameters. For a given inductance value ($L = 1.2$ mH in this case), it is easy to find a theoretical model of the inductor, including its self-capacitance C , which closely resembles the measured impedance. Using the equivalent circuit of the inductor, outlined in Figs. 2a and 3a, a suitable value for C can be selected, such that the theoretical impedance fits the measured one, as shown in Fig. 5. The low frequency impedance is mostly affected by the *equivalent series resistance* (ESR), denoted by R_s . The peak at the resonant frequency, on the other hand, is determined by the *equivalent parallel resistance* (EPR), which is denoted by R_p . Without R_p the theoretical impedance would peak at infinity.

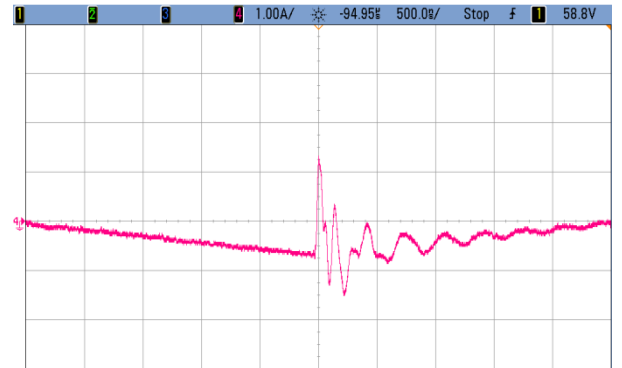


Figure 4. Inductor current waveform at switch turn-on.

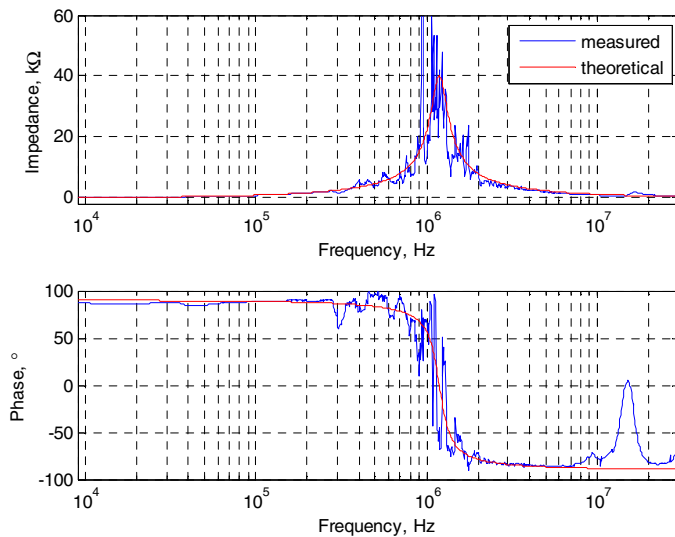


Figure 5. Measured impedance of inductor No. 2 and impedance of the theoretical model in Figs. 2a and 3a with $C = 15$ pF, $R_s = 5$ mΩ and $R_p = 40$ kΩ.

Depending on the frequency range and the characteristics of any particular inductor the measurements may show multiple resonances, which cannot be modeled with the equivalent circuit in Figs. 2a and 3a.

E. Self-Capacitance Measurement Results

The parasitic capacitance of the two inductors was measured according to the methods described above and the results are given in Table I. The parasitic capacitance of inductor No. 1 ranges from 155 pF to 167.5 pF and that of inductor No. 2 is between 10.88 pF and 20.45 pF. Whatever the accuracy of these methods may be, the new winding method, which was used for inductor No. 2, reduced the self-capacitance at least 8 times. This noticeable reduction of the parasitic capacitance shows that the layer-to-layer capacitance is the most significant part of the total self-capacitance. The turn-to-turn capacitances in a given winding layer are actually in series and contribute slightly to the total self-capacitance. On the other hand, the parasitic capacitances between different layers are in parallel and add to each other. Therefore, the most effective way to reduce the total parasitic capacitance is to minimize the layer-to-layer capacitance, which is exactly what the proposed winding method does.

TABLE I. MEASURED PARASITIC CAPACITANCE

Method	Inductor		No. 1	No. 2
	f_r	kHz		
A	C	pF	167.5	15.1
	C	pF	155.3	10.88
B	Q	nC	100.1	12.28
	C	pF	166.9	20.45
C	f_r	kHz	346.4	1186
	C	pF	165	15

When comparing the above measurement methods, it can be said that methods A and D must be the most reliable ones, but they rely on certain type of equipment - variable frequency generator for method A and a VNA for D. Method B requires only a DC voltage source and two or more semiconductor switches, but it is time consuming. Moreover, it cannot be very accurate, given the fact that the self-capacitance values are in the pF range, which is close to the parasitic capacitance values of the voltage probe and the capacitance tolerances of the switches.

Method C has the advantage that it can be used “on-line”, i.e. while the converter operates. Unfortunately, it too cannot be very accurate because it depends on the current probe, its location, and other parasitic elements that play a role in the switching process.

IV. ROLE OF THE PARASITIC CAPACITANCE OF THE INDUCTOR IN A BOOST CONVERTER

The role of the parasitic capacitance of the inductor in a boost converter was studied by comparing the converter performance when operating with each of the above described inductors, No. 1 and No. 2. The parameters of the boost converter are given in Table II.

TABLE II. BOOST CONVERTER PARAMETERS.

Parameter	Value
Input/output voltage	300 V / 600 V
Rated power	2 kW
Load current	$I_L = 3.3$ A
Duty cycle	0.5
Switching frequency	100 kHz
Inductor	$L = 1.2$ mH / 8 A
Input capacitor	4.7 μF / 400 V
Output capacitor	40 μF / 700 V
Device ratings	1.2 kV / 15 A (SiCED)
SiC Schottky diode	1.2 kV / 5 A

Each time the switch in the boost converter turns-on, the parasitic capacitance of the inductor must be charged to the input voltage, which causes a positive spike in the inductor current (Fig. 4). The same spike can be seen also in the switch current. Fig. 6a shows the turn-on waveforms of the JFET with inductor No. 1. The current spike is much larger than that in Fig. 6b, which shows the switch turn-on waveforms with inductor No. 2.

During turn-off, the parasitic capacitance of the inductor must be charged in the opposite direction, which is why the spike at turn-off is negative.

The larger the self-capacitance of the inductor, the larger the spikes at turn-on and turn-off, and longer the duration of the transient process after the switching. The turn-on and turn-off spikes trigger oscillations, like in the previously discussed method B for measuring the self-capacitance of the inductor. Converters with SiC devices may operate at frequencies of

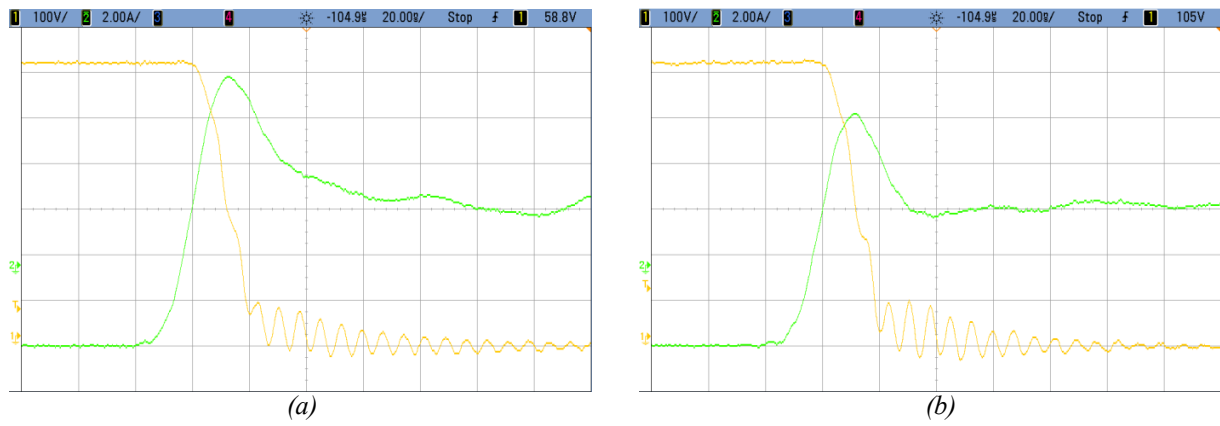


Figure 6. Transistor voltage (yellow) and current (green) waveforms during turn-on with inductor: *a)* No. 1 (high C), and *b)* No. 2 (low C).

hundreds of kHz. Any inductor with $L > 1$ mH and self-capacitance just over 100 pF will resonate at frequency below 500 kHz. When the switching frequency is so close to the *self-resonant frequency* (SRF) of the inductor, the boost converter operation worsens. Resonances within the inductor itself or between the inductor and the parasitic elements of the semiconductor devices are possible. Fig. 7*a* shows such resonant behavior during steady-state operation of the boost converter with inductor No. 1. This is not the case with inductor No. 2 (Fig. 7*b*). The initial spikes in this case are very

small and the oscillations decay very quickly. The only difference between the two cases is the self-capacitance of the inductor, which is much smaller in the 2nd case, and therefore, the SRF of the inductor is much higher (above 1 MHz).

The inductor current spikes and oscillations are not desirable because they increase the electromagnetic emissions, the inductor losses, and the switching losses as well. Fig. 9 shows the instantaneous power during turn-on in the two cases. As expected, the switching energy with inductor No. 2 is lower than the switching energy with inductor No. 1, because of the smaller current spikes and faster switching transient. This result was confirmed by the power-loss measurements with a power analyzer. Replacing inductor No. 1 with inductor No. 2 in the boost converter decreased the power losses from 31.6 W to 26.7 W, which is a reduction of 15.5 %.

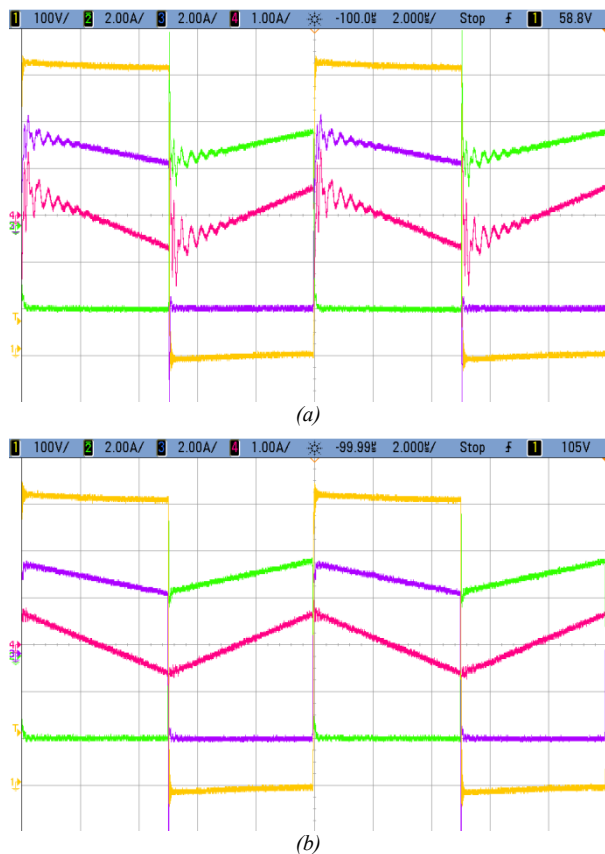


Figure 7. Waveforms of: transistor voltage (yellow) and current (green), diode current (violet), and inductor current (red), during steady-state operation with inductor: *a)* No. 1, and *b)* No. 2.

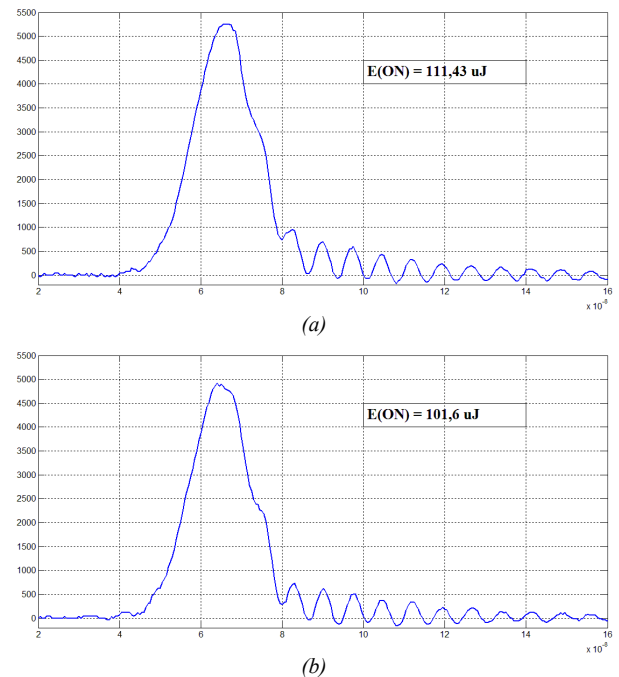


Figure 8. Waveforms of the instantaneous power during turn-on with inductors: *a)* No. 1, and *b)* No. 2.

V. CONCLUSIONS

The parasitic capacitance of an inductor and its impact on the operation of a boost converters with normally-on SiC JFETs were discussed in this paper. Two inductors with the same core and number of turns were compared. The first inductor had conventional winding with two layers and the second one had an air-gap between its winding layers. The parasitic capacitance of the inductors was measured by four methods. The total parasitic capacitance was reduced more than 8 times, although the proposed winding method minimizes only the layer-to-layer parasitic capacitance. This is because the layer-to-layer capacitance is the largest part of the total parasitic capacitance of the inductor.

The two inductors were tested in a 2 kW, 100 kHz boost converter with normally-on SiC JFET. The converter with conventionally winded inductor had larger oscillations after each switching, which can lead to larger electromagnetic emissions, unstable operation, and larger converter losses. The low-capacitance inductor had very small oscillations during the switching transients and approximately 16 % less losses. This shows that minimizing the parasitic capacitance of the inductor is worthwhile – it improves the switching performance and the efficiency of the boost converter.

ACKNOWLEDGMENT

This work was supported by the European Union in the framework of the European Social Fund through the Warsaw University of Technology Development Programme, realized by the Center for Advanced Studies.

REFERENCES

- [1] P. Friedrichs, "Silicon carbide power semiconductors – new opportunities for high efficiency", 3-rd IEEE Conf. on Industrial Electronics and Applications ICIEA 2008, pp. 1770-1774.
- [2] P. Friedrichs P. et al., "The vertical silicon carbide JFET – a fast and low loss solid state power switching device", 9th European Conference on Power Electronics and Applications, EPE 2001
- [3] I. Sankin, et al., "Normally-off SiC VJFETs for 800 V and 1200 V power switching applications", 20th International Symposium on Power Semiconductor Devices and ICs, pp. 260-262, 2008.
- [4] A. Ritenour, D. C. Sheridan, V. Bondarenko, J. B. Casady, "Saturation current improvement in 1200 V normally-off SiC VJFETs using non-uniform channel doping", 22nd International Symposium on Power Semiconductor Devices & ICs, pp. 361-364, 2010.
- [5] A. Lindgren, M. Domeij, "1200V 6A SiC BJTs with very low VCESAT and fast switching", 6th International Conference on Integrated Power Electronics Systems, pp. 1-5, 2010.
- [6] J. A. Cooper, M. R. Melloch, R. Singh, A. Agarwal, J. W. Palmour, "Status and prospects for SiC power MOSFETs", IEEE Transactions on Electron Devices, vol. 49, No. 4, pp. 658-664, April 2002.
- [7] J. Cass Callaway, et al., "Evaluation of SiC JFETs for a three-phase current-source rectifier with high switching frequency", 22nd Annual IEEE Applied Power Electronics Conference, APEC 2007, pp. 345–351.
- [8] T. Friedli, S. D. Round, D. Hassler, J. W. Kolar, "Design and performance of a 200-kHz All-SiC JFET current DC-link back-to-back converter", IEEE Transactions on Industry Applications, Vol. 45, Iss. 5, pp. 1868 – 1878.
- [9] A. M. Abou-Alfotouh, A. V. Radun, Hsueh-Rong Chang, C. Winterhalter, "A 1-MHz hard-switched silicon carbide DC-DC converter", IEEE Transactions on Power Electronics, Vol. 21, Iss. 4, pp. 880–889, July 2006.
- [10] J. Biela, M. Schweizer, S. Waffler, J. W. Kolar, "SiC vs. Si-evaluation of potentials for performance improvement of inverter and DC-DC converter systems by SiC power semiconductors", IEEE Transactions on Industrial Electronics, Vol. 58, Iss. 7, pp. 2872-2882, July 2011.
- [11] M. S. Mazzola, R. Kelley, "Application of a normally off silicon carbide power JFET in a photovoltaic inverter, Applied Power Electronics Conference and Exposition, APEC'09, pp. 649–652, 2009.
- [12] G. Tolstoy, D. Pefitsis, J. Rabkowski, and H.-P. Nee, "Performance tests of a $4,1 \times 4,1 \text{ mm}^2$ SiC LCVJFET for a DC/DC boost converter application", Proc. European Conference on Silicon Carbide and Related Materials, ECSCRM 2010, Oslo, Norway, pp. 722-725, 29 August - 2 September 2010.
- [13] D. Kranzer, C. Wilhelm, F. Reinert, B. Burger, "Application of normally-off SiC-JFETs in photovoltaic inverters", Proceedings (CD) of 13th European Conference on Power Electronics and Applications, EPE, 2009.
- [14] J. Rabkowski, R. Barlik, "Three-phase inverter with SiC JFETs and schottky diodes", Przegląd Elektrotechniczny (Electrical Review), No. 11a, pp. 116-119, 2010.
- [15] J. Rabkowski, M. Zdanowski, R. Barlik, "Silicon carbide inverter with two series Z-networks", 20th International Symposium on Industrial Electronics, ISIE 2011, pp. 372-377.
- [16] D. Pefitsis, J. Rabkowski, G. Tolstoy, H.-P. Nee, "Experimental comparison of dc-dc boost converter with SiC JFETs and SiC bipolar transistors", Proceedings (CD) of 14th European Conference on Power Electronics and Applications, EPE'2011.
- [17] A. Massarini, M. K. Kazimierzczuk, "Self-capacitance of inductors", IEEE Trans. on Power Electronics, Vol. 12, No. 4, 1997, pp. 671-676.
- [18] L. Dalessandro, F. da Silveira Calvalcante, J. W. Kolar, "Self-capacitance of high voltage transformers", IEEE Trans. on Power Electronics, Vol. 22, No. 5, pp. 2081-2092, 2007.
- [19] P. Ranstad, H.-P. Nee, "On the distribution of AC and DC winding capacitances in high-frequency power transformers with rectifier loads", IEEE Trans. on Power Electronics, Vol. 58, No. 5, pp. 1789-1798, 2011.
- [20] H. Y. Lu, J. G. Zhu, S. Y. Hui, "Experimental determination of stray capacitances in high frequency transformers", IEEE Trans. on Power Electronics, Vol. 18, No. 5, pp. 1105-1112, 2003.
- [21] H. Y. Lu, J. G. Zhu, V. S. Ramsden S. Y. Rhui, "Measurement and modeling of stray capacitances in high frequency transformers", Power Electronics Specialists Conference, PESC'99, pp. 763-768, 1999.
- [22] V. C. Valchev, A. Van den Bossche, "Inductors and Transformers for Power Electronics", Chapter 11.6.2 Measurement of the Equivalent Parallel Capacitance of Winding, pp. 405-406
- [23] G. Grandi, M. K. Kazimierzczuk, A. Massarini, U. Reggiani, "Stray capacitances of single-layer solenoid air-core inductors", IEEE Trans. on Industrial Electronics, Vol. 35, No. 5, pp. 1162-1168, 1999.
- [24] Y. J. Kim, M. G. Allen, "Integrated solenoid-type inductors for high frequency applications and their characteristics", Electronics Components and Technology Conference, pp. 1247-1252, 1998.
- [25] Q. Yu, T. W. Holmes, "Stray capacitance modeling of inductors by using finite element method", Electromagnetic Compatibility, pp. 305-310, 1999.